

Docket No.: GR 98 P 2078

**THE UNITED STATES PATENT AND TRADEMARK OFFICE**

RCE of Applic. No. : 09/124,288 Confirmation No.: 6541  
Inventor : Jens Barrenschenn et al.  
RCE Filed : December 11, 2003  
TC/A.U. : 2155  
Examiner : Patrice Winder

#23  
LDT  
3-17-04

**RECEIVED**

DEC 1 9 2003

Technology Center 2100

Docket No. : GR 98 P 2078  
Customer No. : 24131

Hon. Commissioner for Patents  
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT**  
**UNDER 37 C.F.R. 1.97(b)(4)**

Sir:

In accordance with 37 C.F.R. 1.97(b)(4), copies of the following patents and/or publications are submitted herewith:

U.S. Patent No. 4,158,235 (Call et al.), dated June 12, 1979;

"Software-Controlled Wrap-Around Buffer", IBM Technical Disclosure Bulletin, Vol. 28, No. 12, May 1986, pp. 5314-16;

Tam-Anh Chu et al.: "Design of VLSI Asynchronous FIFO Queues for Packet Communication Networks", XP-000756967, IEEE, 1986, pp. 397-400;

S.G. Tzafestas: "On the Design of Multi-Input Periodic-Block-Output Buffers with Binomial Feedback", XP-002123624, pp. 120-125.

Respectfully submitted,

For Applicants

Date: December 11, 2003  
Lerner And Greenberg, P.A.  
Post Office Box 2480  
Hollywood, FL 33022-2480  
Tel: (954) 925-1100  
Fax: (954) 925-1101  
/bb

**RALPH E. LOCHER**  
**REG. NO. 41,947**

FORM PTO-1449 (SUBSTITUTE)

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

Attorney Docket No.:

GR 98 P 2078

RCE of Applic. No.

09/124,288

Applicant

Jens Barrenschenn et al.

RCE Filing Date

December 11, 2003

Group Art Unit

2155

INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT  
(37 CFR 1.98(b))

## U.S. PATENT DOCUMENTS

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A	4,158,235	06/79	Call et al.			
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						

RECEIVED

DEC 18 2003

Technology Center 2100

## FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES / NO
	J						
	K						
	L						
	M						
	N						

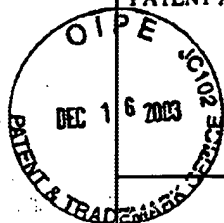
## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	O	"Software-Controlled Wrap-Around Buffer", IBM Technical Disclosure Bulletin, Vol. 28, No. 12, May 1986, pp. 5314-16.
	P	Tam-Anh Chu et al.: "Design of VLSI Asynchronous FIFO Queues for Packet Communication Networks", XP-000756967, IEEE, 1986, pp. 397-400.

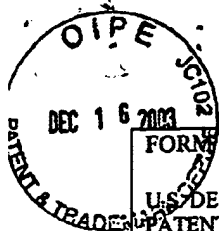
EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



#23



FORM PTO-1449 (SUBSTITUTE) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE  INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))	Attorney Docket No.: RCE of Applic. No. GR 98 P 2078 09/124,288  Applicant Jens Barrenschenn et al.  RCE Filing Date Group Art Unit December 11, 2003 2155
--	---

## U.S. PATENT DOCUMENTS

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A						
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						

RECEIVED

DEC 19 2003

Technology Center 2100

## FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES   NO
	J						
	K						
	L						
	M						
	N						

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	O	S.G. Tzafestas: "On the Design of Multi-Input Periodic-Block-Output Buffers with Binomial Feedback", XP-002123624, pp. 120-125.
	P	

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.